Niraj Hariyani

Varanasi, India
+91-9518714332 nirajhariyani3214@gmail.com linkedin.com/in/niraj-hariyani github.com/fulllofhope

Education

Indian Institute of Technology (BHU), Varanasi **July 2024 – May 2028**
Bachelor of Technology in Electronics Engineering *CGPA: 9.19/10.0*

Relevant Coursework

- Digital Electronics
- Verilog HDL
- Computer Architecture
- Signals and Systems
- Analog Communications
- Data Structures
- Analog Electronics
- Solid State Devices

Projects

FPGA-Based FFT Engine for Edge Detection | *Verilog, Vivado, Xilinx Zynq-7000* **Jan 2026 – Apr 2026**

- Designed a fully pipelined 1024-point Radix-2 DIF SDF FFT/IFFT engine in Verilog with Ping-Pong bit-reversal buffers, deployed on Xilinx Zynq-7000 SoC via AXI4-Stream DMA, achieving timing closure at 70 MHz
- Implemented Q1.15 fixed-point arithmetic with convergent rounding and saturation, achieving 2.85% MAPE against double-precision floating-point reference, utilizing only 5 BRAMs and 42 DSP slices on the FPGA fabric.
- Built a configurable circular High-Pass Filter with wrapped-distance combinational masking and hardware IFFT conjugation, zeroing DC-lobe bins within a cutoff radius to isolate high-frequency edge content

AXI Lite DMA Controller with FIFO Buffering | *Verilog, AMBA AXI4 Protocol* **Feb 2026**

- Designed an AXI4-Lite DMA Controller with parallel Read/Write FSMs, achieving timing closure at 170 MHz.
- Integrated a 16-depth, 32-bit synchronous FIFO to decouple AXI channels and absorb memory latency mismatches.
- Implemented an unaligned transfer engine for byte extraction and 32-bit word assembly from non-aligned addresses.
- Ensured aligned 32-bit word writes to destination, dropping incomplete bytes for strict AXI4-Lite compliance.

CipherStream-128X: AES-128 Hardware Accelerator | *Verilog* **Mar 2026**

- Designed a pipelined AES-128 engine in Verilog with 10 pipeline stages, encrypting one 128-bit block per clock cycle
- Implemented SubBytes, ShiftRows, MixColumns, AddRoundKey across a pipelined datapath per NIST FIPS-197
- Built a fully combinational key expansion unit generating all 11 AES round keys from a single 128-bit key

Achievements & Certifications

- **SKY130 Silicon Tapeout:** Architected the front-end for a 64-point SDF FFT hardware accelerator, successfully taped out on the open-source SKY130 process via Tiny Tapeout, marking the first fabricated chip from IIT (BHU)
- **FPGA Training Certification:** Completed an intensive 4-day training by CoreEL Technologies at IIT (BHU), covering Static Timing Analysis (STA), synthesis optimization, and High-Level Synthesis (HLS) for Zynq MPSoC
- **Finalist, 5G Hackathon '26:** Proposed an innovative spectral mapping solution utilizing a custom 2D-FFT hardware architecture (ARGUS) to efficiently share data across 5G bands
- **Academic Excellence:** Achieved a 99.33 percentile in MHT-CET (State Engineering Entrance Examination), ranking among the top candidates out of 400,000+ participants across Maharashtra

Technical Skills

Languages: Verilog HDL, Python, C, C++
Developer Tools: Vivado, GTK Wave, Proteus, LTSpice, VS Code
Technologies/Frameworks: Linux, GitHub

Leadership / Extracurricular

Student Alumni Interaction Cell **June 2026 – Present**
Convener *IIT (BHU), Varanasi*

- Led a 70+ member team directing the institute alumni relations and managing extensive student-alumni initiatives
- Served as Event Executive for Confluentia 2025, the institute's industry connect event, drawing 2000+ attendees
- Organized 5-hour technical workshops alongside industry partners CISCO and Ati Motors, engaging 170+ students
- Spearheaded the Student Alumni Mentorship Program, connecting 800+ mentees with 200+ mentors, across 12 domains
- Contributed to 3+ editions of the institute's Alma Communiqué newsletter, reaching an average 4000+ readership